Nonlinear Control…

The following parameters can be programmed in the **Nonlinear Control** dialog:

- Active Transient Response (ATR) parameters to reduce undershoot or overshoot excursions during transient load events
- Frequency Active Transient Response (FATR) parameters to improve transient response over output load frequency, especially for transient loads at beat frequency
- Dynamic VID (DVID) parameters to optimize the VR's response to the SetVID_Fast/Slow/Decay commands
- Non-Linear parameters to gain more undershoot or overshoot margin at high load repetition frequency
- Feed forward parameters to gain faster response during the specific cases listed below or variable case as below

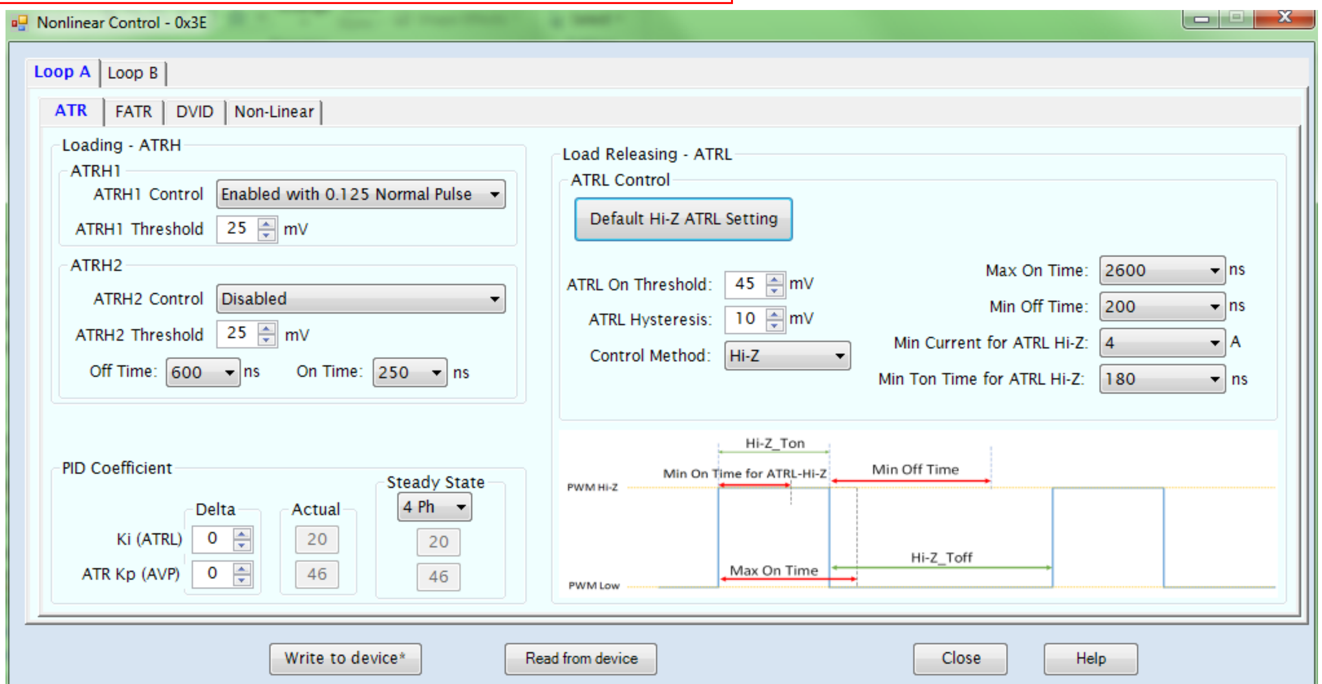
Only enable the ATR functions if adjusting PID alone can not meet the undershoot and overshoot requirements

–ATR control mechanisms are driven by comparators and programmable thresholds

–The response is non-linear and may add jitter at the output

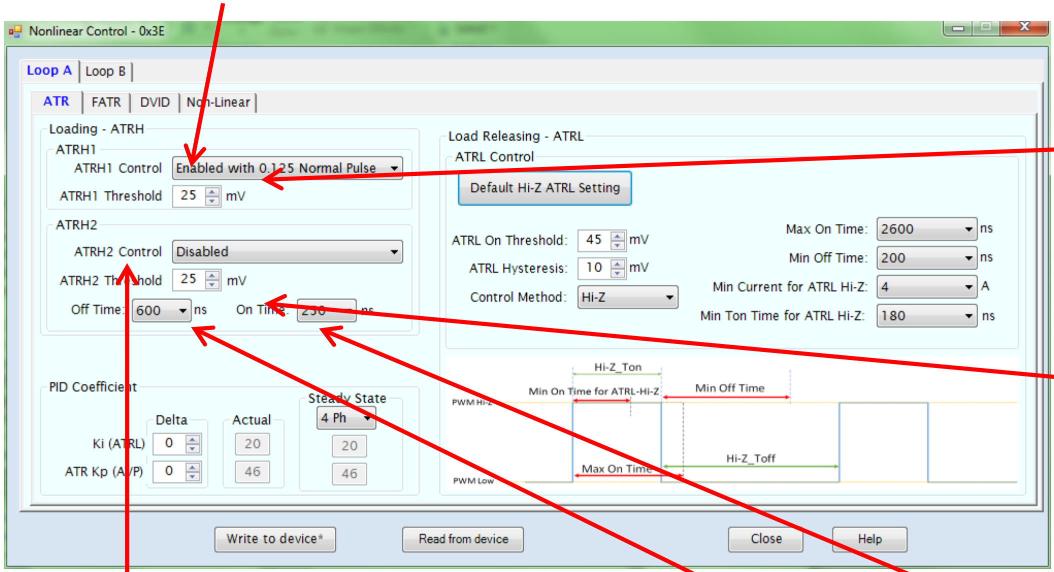
– The thresholds should be at least 5mV (typically 10mV) wider than the measured steady state ripple voltage

– If ATR has to be enable, the PID should be made less aggressive ☐ start by adjusting(lower) Kd and Kfp terms



Nonlinear Control… ATR

ATRH1 Control
–Use to program the strength of the ATRH1 control
–A wider pulse width corresponds to a stronger ATRH1 control
–Disable: No ATRH1 control
–Enabled with 0.50/0.375/0.25/0.125 Normal Pulse: ATRH1 control is enabled. The normal pulse width is decided by the feedback loop control and ATRH1 will be fired in 0.50/0.375/0.25/0.125 normal pulse width
–Recommended starting point is 0.25 of normal pulse if ATRH1 is needed. Stronger ATRH control reduces the undershoot of VOUT but will increase ring-back.



ATRH1 Threshold
–ATRH1 control threshold
–The smaller the threshold, the stronger the ATRH1 response because of the increased likelihood that ATRH1 will be triggered
–It is recommended that the threshold not be too close to the steady-state ripple size, otherwise ATRH pulses can be falsely fired during normal regulation. Select a threshold at least 10mV higher than measured VOUT switching ripple.

ATRH2 Threshold–ATRH2 control threshold
–Similar to ATRH1 Threshold
– Recommended to set > ATRH1 Threshold

On Time
–On time (PWM high duration) of the ATRH2 pulse when ATRH2 Control is set to Enabled with Pulse Control
–If ATRH2 On time is too narrow, it could be swallowed by the driver and then provide little or no help in reducing undershoot
-If ATRH2 On time is too large, it could saturate output inductor. It can also make the PWM width too wide and be limited by the maximum duty cycle setting.
-Select ATRH2 pulse in the range of 100ns to 200ns and select a much longer Off time (>800ns) for robust ATRH2 behavior

ATRH2 Control . Only use if ATRH1 is not enough.

–Disabled: no ATRH2 control,
–Enabled with Pulse Control: ATRH2 pulse width is programmed by the Off Time and On Time

Off Time
–Off time (PWM low duration) of the ATRH2 pulse when ATRH2 Control is set to Enabled with Pulse Control

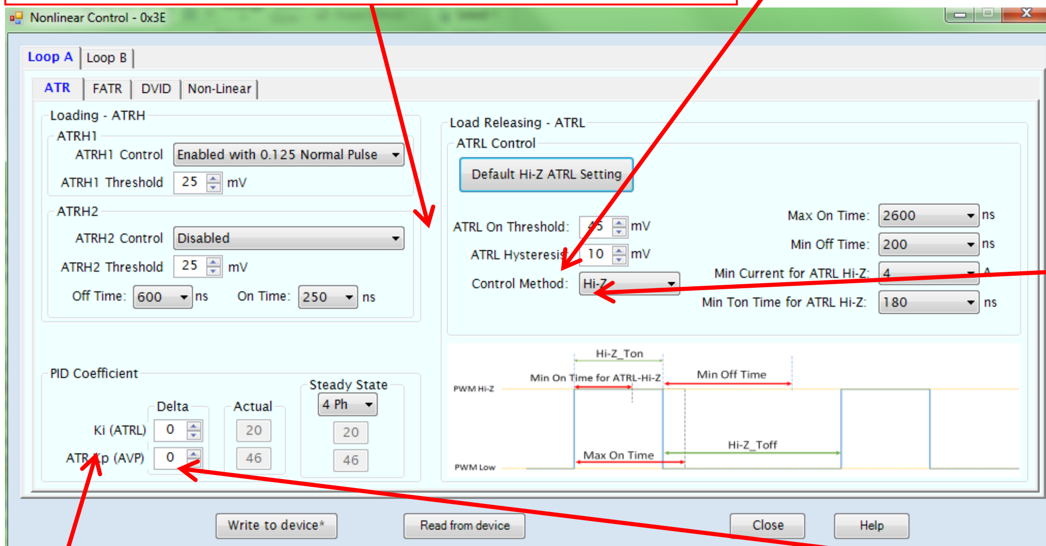
Nonlinear Control... ATR

ATRL On Threshold
–ATRL will be engaged if the VOUT overshoot exceeds the target VOUT plus this threshold
–Recommended not to set smaller than the switching ripple amplitude, otherwise it will be falsely fired in the steady state

ATRL On Hysteresis
–Prevents ATRL window chattering and hence stressing FET drivers
–Recommended value is 10mV

Control Method
–Disabled: Disable ATRL
–Hi-Z: Low side FET is off, uses Body diode
- Low side on: FET turns on when ATRL window is active
–Recommended to be in Hi-Z if ATRL needs to be enabled

•When both high side FET and low side FET are off, the positive current will go through the low side body diode
•Compared to the path through low side FET, the low side body diode will cause a larger voltage drop across the low side FET and be able to reduce the positive inductor current sooner, thereby more effectively reduce the overshoot



Ki (ATRL)
–Delta: This will reduce Ki when the ATRL window is active regardless of ATRL function is enabled/disabled. When the ATRL window is active, less error Voltage signal will be accumulated by the integrator which allows the average VOUT to be shifted up during high frequency transients that relieves some stress on meeting the undershoot specifications.
–Actual: Calculated value based on the Delta and Steady State
–Steady State: Steady state Ki value for different number of phases

ATR Kp (AVP)*
–Delta: Kp(avp) index when ATR is detected
–Actual: Calculated value based on the Delta and Steady State
–Steady State: Steady state Kp value for different number of phases

Nonlinear Control… ATR

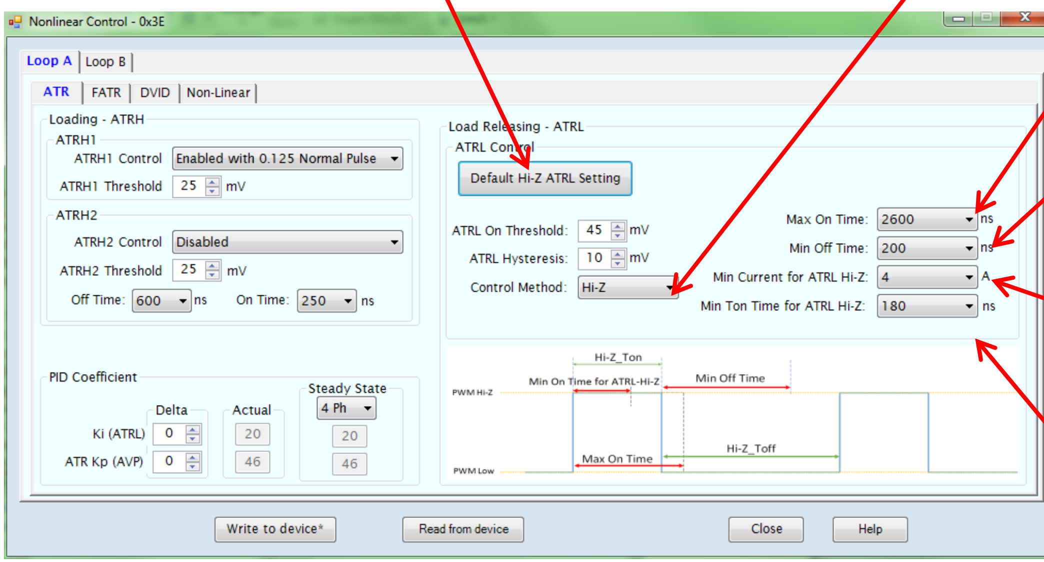
Control Method
–Disabled: Disable ATRL
–Hi-Z: Low side FET is off, uses Body diode
-Low side on: FET turns on when ATRL is active

–Recommended to be in Hi-Z if ATRL needs to be enabled. See description on following slides

Default Hi-Z ATRL setting
Set all the ATRL parameters to a default setting with Hi_Z response

Max Off Time
–Maximum PWM Hi-Z duration in ATRL Hi-Z control mode when the ATRL window is active

Min Off Time
–Minimum PWM low duration in ATRL Hi-Z control mode when the ATRL window is active

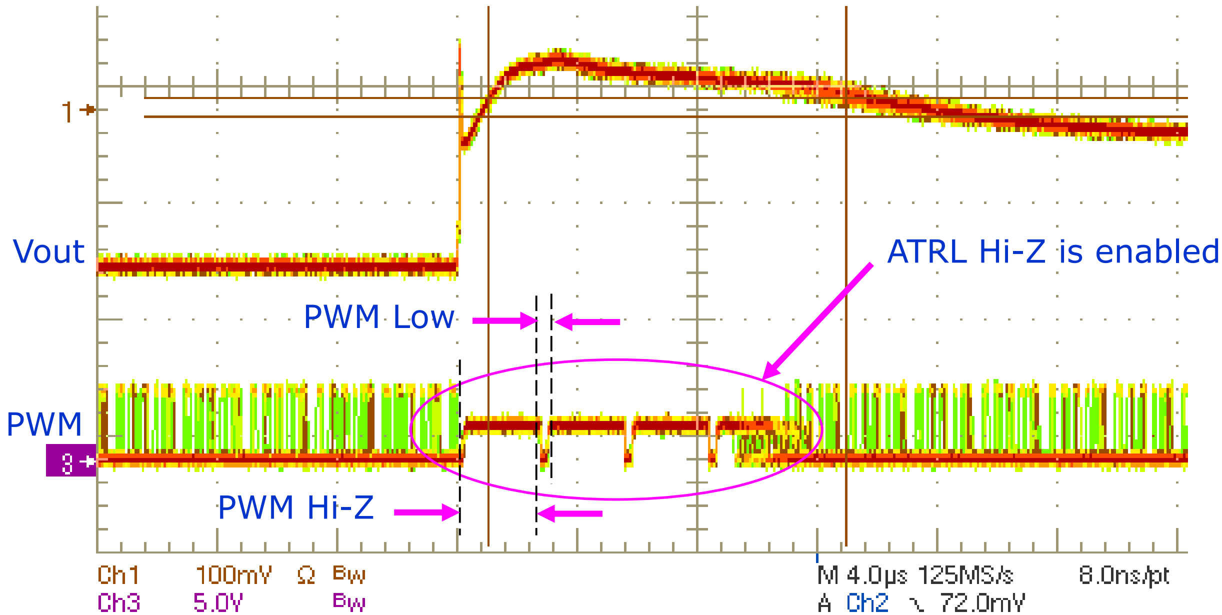


Min Current for ATRL Hi-Z
–Minimum current in ATRL Hi-Z control mode when the ATRL window is active. If the current (per phase) is lower the setting here, the ATRL control mode will become "Low Side ON" See next page for more details

Min Ton Time for ATRL Hi-Z
–Minimum PWM Hi-Z duration in ATRL Hi-Z control mode when the ATRL window is active

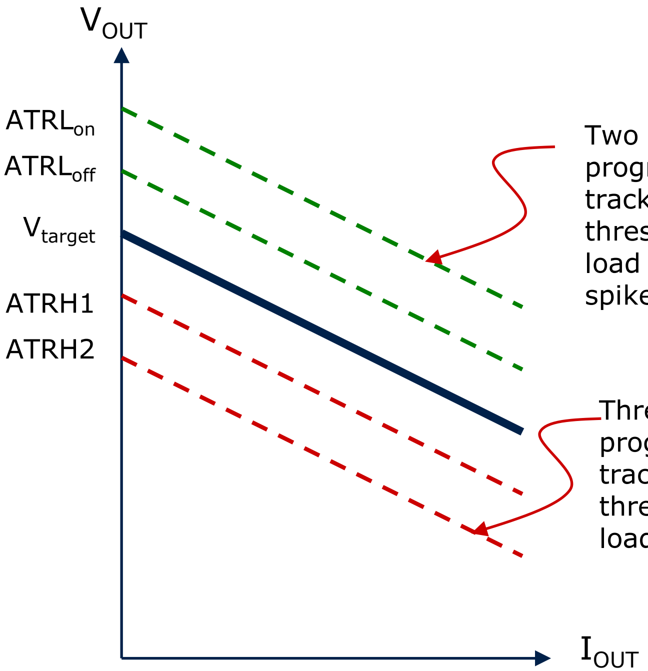
Nonlinear Control... ATR

- **Min Current for ATRL Hi-Z**
- –When the phase current is lower than the setting specified here, the ATRL behavior will be changed from Hi-Z to LSFET on
- –Minimum positive inductor required to sustain Hi-Z state during ATRL
- –When the inductor current falls below this threshold, the low side FET will turn on to continuously discharge the output cap



Nonlinear Control: ATR Overview

- Active Transient Response (ATR) is used to reduce undershoot or overshoot excursions during transient load events
  - ATR**H**: Actively inserts additional pulses (PWM **H**igh pulses) on each phase to minimize undershoot during load step conditions
  - ATR**L**: Actively turns on the low side FET(s) (PWM **L**ow pulses) or forces PWM into tri-state so that the inductor current can go through the low side body diode during load release conditions
- ATR**H** threshold: ATRH will be fired when the droop caused by the load step is above the programmed threshold
  - ATRH1/2 programmable thresholds
- ATR**L** threshold: ATRL will be fired when either of the 2 programmable tracking thresholds are entered during load release spikes
  - ATRLon
  - ATRLoff = ATRLon Hysteresis

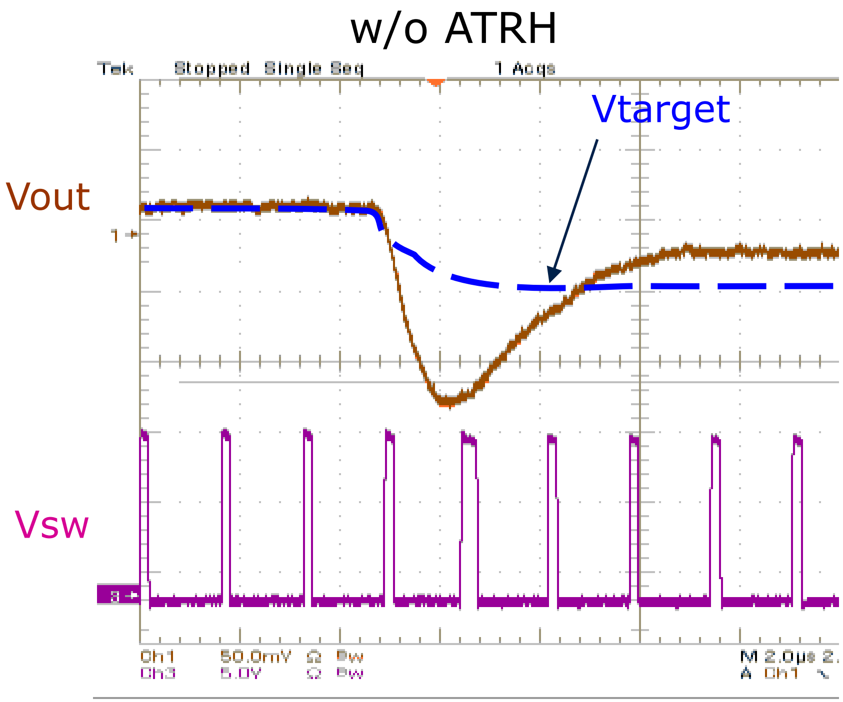


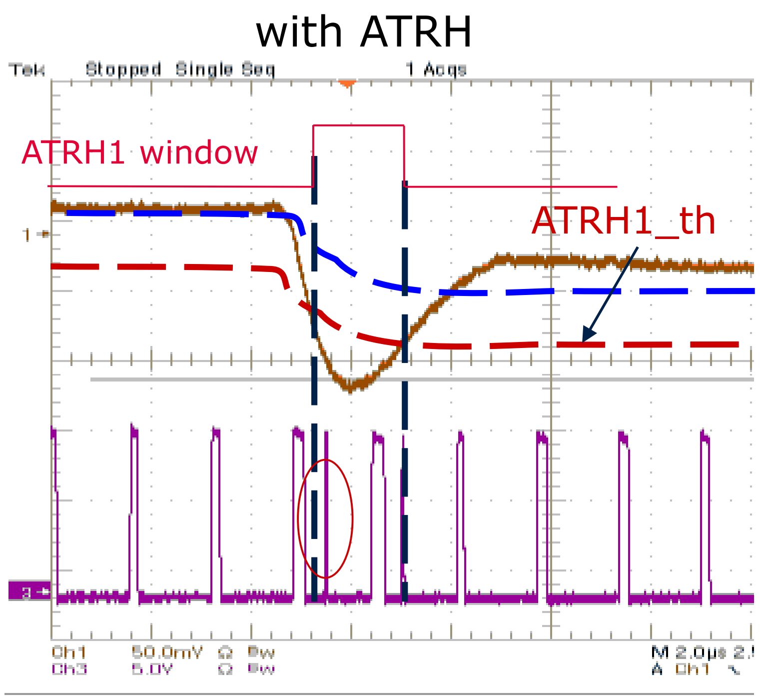
Nonlinear Control: ATRH

- ATRH – undershoot detector
  - Use during positive load steps to enable the additional PWM pulses on top of the regular scheduled PWM pulses controlled by the PID
    - This adds pulses to one or more phases to reduce the V_{OUT} undershoot
  - When V_{OUT} is below the ATRH threshold, the corresponding ATRH window will be activated
  - The firing of ATRH pulses between phases are “scheduled” to prevent inductor saturation
    - The pulse width of the ATRH pulses is controlled by a combination of the PID and the programmable on/off time durations

Nonlinear Control: ATRH

- When the load undergoes a positive step (increased load current), V_{OUT} droops
- When V_{OUT} < ATRH_th, the controller will fire extra PWM pulses to reduce undershoot
  - The ATRH_th is equal to target voltage minus ATRH threshold





Nonlinear Control: ATRL

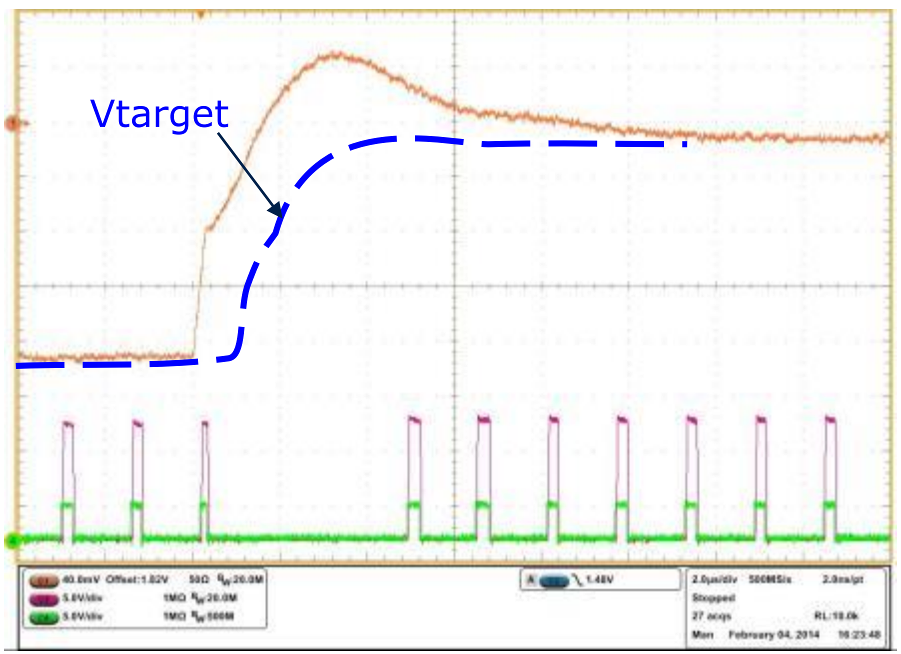
- ATRL – overshoot detector
  - Use during negative load step (load current release) to quickly bring the PWM outputs to a Hi-Z or Low state (depending on what the programmed action is)
    - This turns off the power stage in Hi-Z mode letting current flow through the Body diode to dissipate the energy.
    - Or when in Low Side On mode turns on the low side FET

    to reduce the V_{OUT} overshoot
  - When V_{OUT} is above the ATRLon threshold, the ATRL window will be activated and deactivates once V_{OUT} drops below ATRLoff threshold.
  - If ATRL is disabled normal switching will continue and the PWM pulses will be shorter during the load release compared to when ATRL is on and either PWM pulses are supressed (LowSide FET on) or High Impedance (Hi-Z) to force current through the FET body diode.

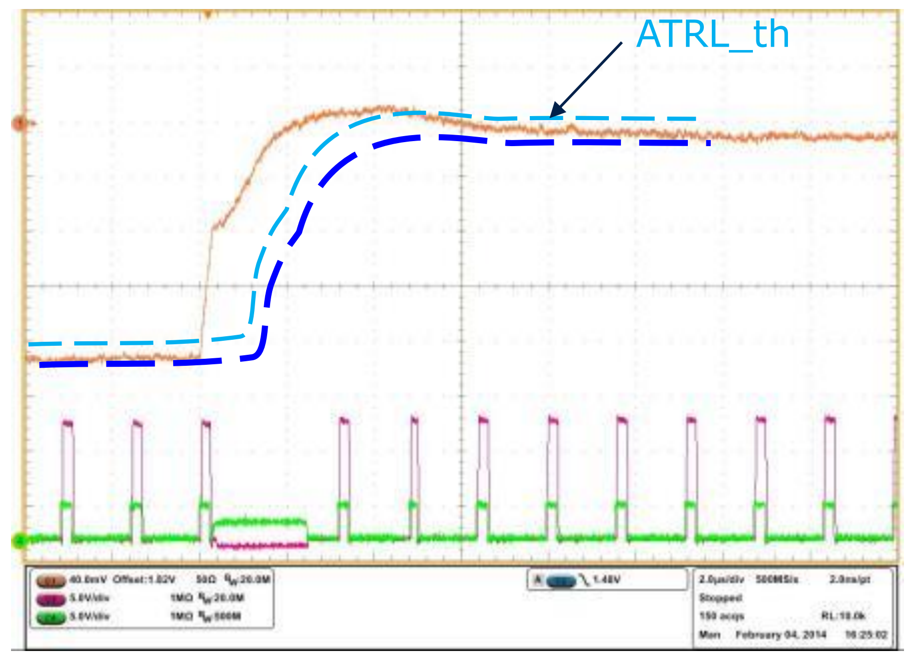
Nonlinear Control: ATRL

- When the load is released, V_{OUT} overshoots due to excess energy in the inductor being transferred to the output capacitors
- When V_{OUT} > ATRL_th, activating a PWM Hi-Z or Low Side On mode will attempt to dissipate some excess energy to reduce overshoot
  - ATRL_th is target voltage plus ATRL on threshold

w/o ATRL

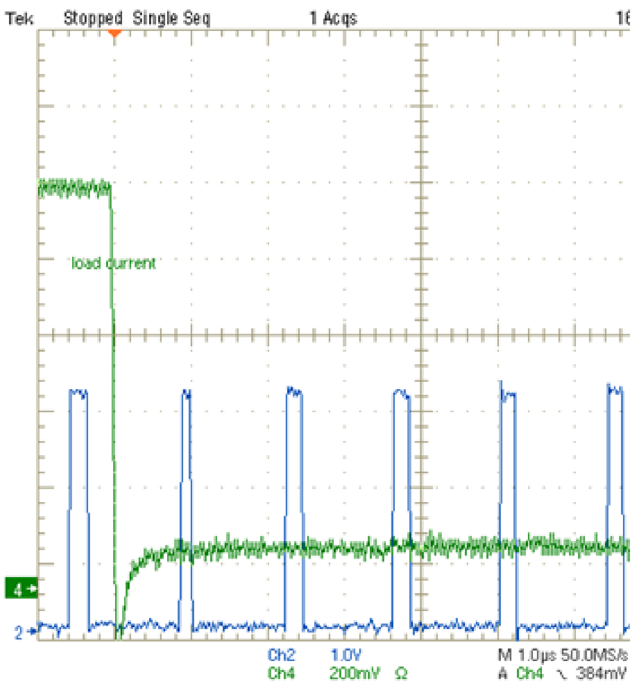


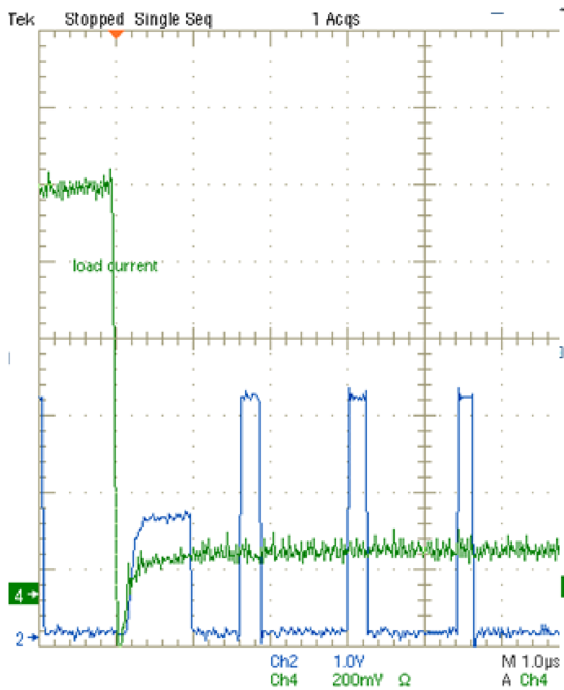
with ATRL

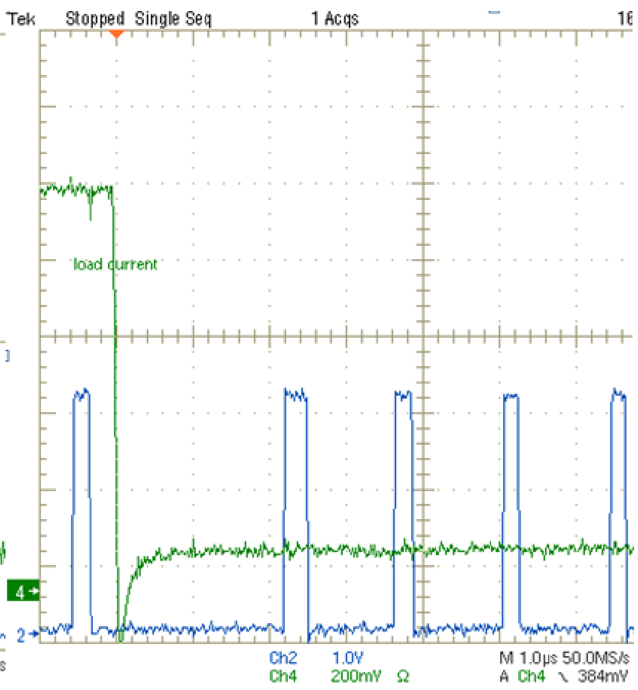


Nonlinear Control: ATRL

- The three settings for ARTL will treat the PWM signal differently
- Disabled Hi-Z Low Side on





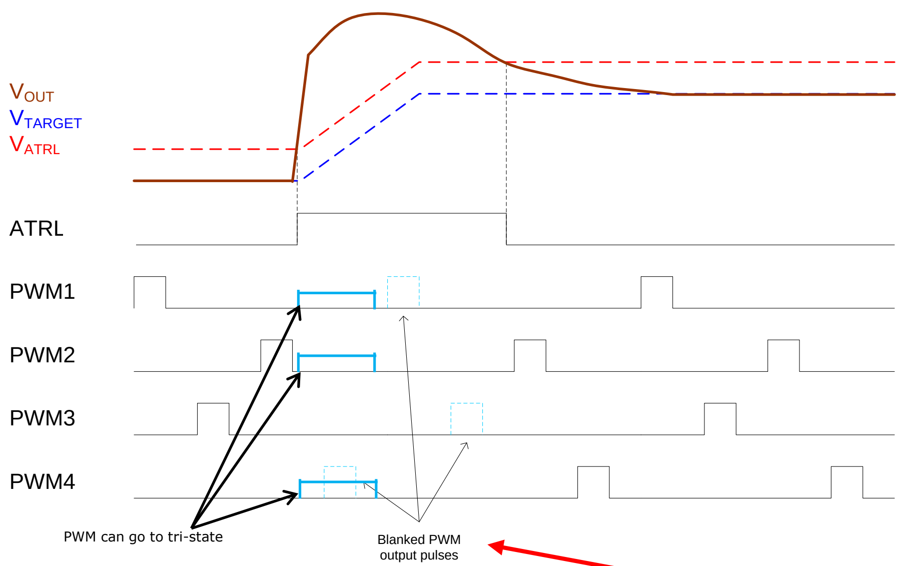


Disabled=ATRL is not active at all. PWM pulses continue

Hi-Z= Let the circulating current go through the body diode of the bottom FET

Low Side On= FET is on and let inductor current circulate through bottom FET and pulses are skipped.

Nonlinear Control: ATRL



Hi-Z

All PWM phases tri-state at the same time to all phases until Vout falls below ATRL threshold voltage

Low Side on

PWM pulses are blanked the whole time Vout is above ATRL threshold voltage

Disabled

PWM pulses are continuing during the load release.

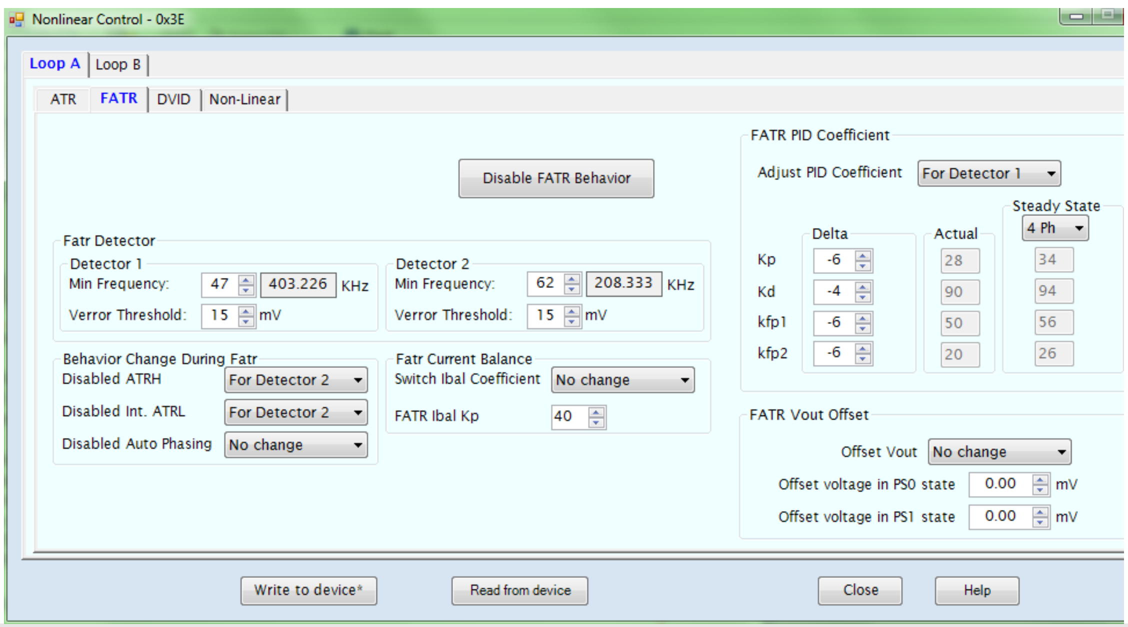
PWM pulses may be blanked for high Vout overshoot depending on how fast PID regulation reacts

Nonlinear Control: ATR Recommendations

- Only enable the ATR functions if adjusting PID alone can not meet the undershoot and overshoot requirements
  - ATR control mechanisms are driven by comparators and programmable thresholds
  - The response is non-linear and may add jitter at the output
- The thresholds should be at least 5mV (typically 10mV) wider than the measured steady state ripple voltage
- If ATR has to be enable, the PID should be made less aggressive → start by adjusting Kd and Kfp terms

Nonlinear Control...FATR

›FATR can improve transient response over output load frequency, especially for transient loads at beat frequency.
›FATR is made up of 3 independent load frequency detectors and adjustment controls that activate when the target load frequencies are detected.
›Only enable FATR if adjusting PID and ATR together still cannot meet the undershoot and overshoot requirements.
›Recommended FATR settings are the default settings when FATR is required.
›Recommended FATR settings for manual optimization of the FATR settings
–Step 1: Determine the oscillation frequency
–Step 2: Determine the cause of the oscillation
- •If it is due to ATR, disable ATR at a frequency that is slightly below the frequency determined in step 1
- •If it is due to an aggressive PID, lower the bandwidth at a frequency that is slightly below the frequency determined in step 1
- •If it is due to current balance, increase the current balance Kp coefficient at frequencies above one-fifth of the switching frequency

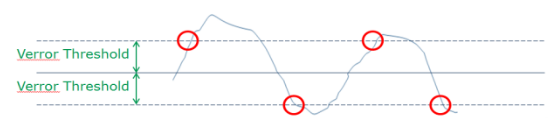


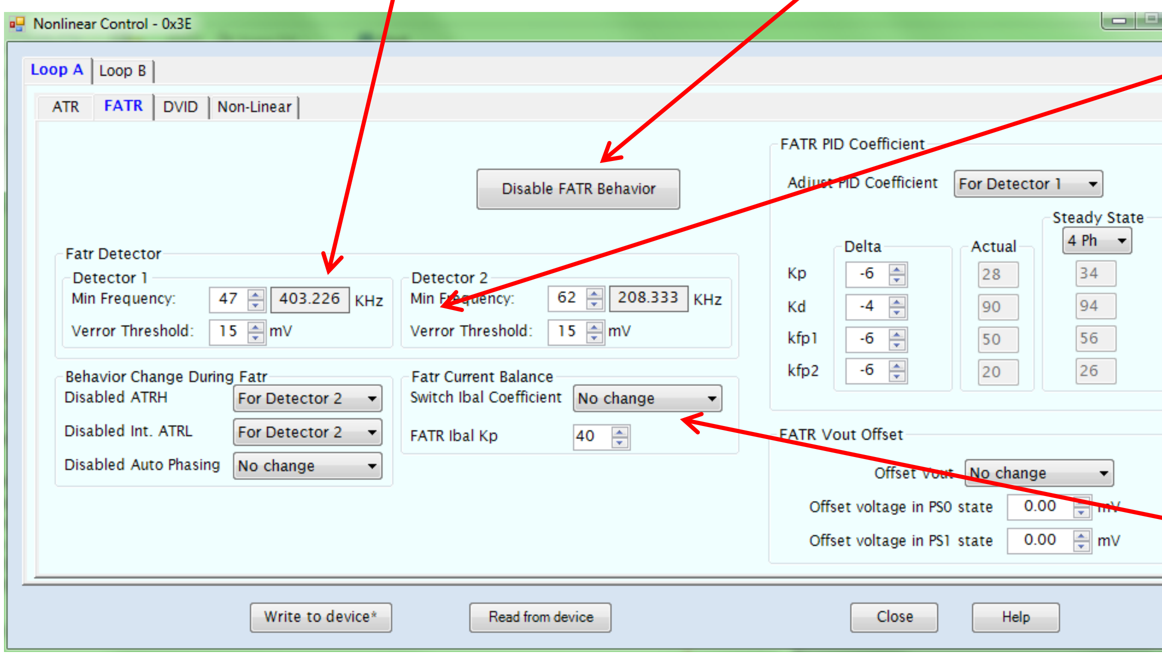
Nonlinear Control...FATR

Disable FATR Behavior / Restore FATR Behavior
Button will toggle the text each time it is clicked
–Selection boxes below will display “No Change” in terms of FATR behavior when disabled

Min. Freq. (Detector 1and 2)
–Minimum load transient frequency for Detector 1 and 2
–A frequency above the specified frequency and an amplitude above Verror Threshold will execute FATR settings.

Verror Threshold (Detector 1 and 2)
–Defines the window which the controller counts the number of crossings above and below the Verror threshold over time to determine the load repetition frequency
–Verror threshold should be greater than the output ripple voltage to avoid false detection.





FATR Current Balance

–The recommended setting is to adjust the current balance parameter Kp (**FATR Ibal. Kp**) to ≥40 at and above one-fifth of the switching frequency to mitigate circulating current

Nonlinear Control...FATR

Behavior Change During FATR: select the desired behavior for various Non-Linear features when the load frequency is above the FATR setting

–*No Change*: no behavior change
–*For Detector 1or 2*: behavior change based on the detector value selected

FATR Current Balance

–The recommended setting is to adjust the current balance parameter Kp (**FATR Ibal. Kp**) to ≥40 at and above one-fifth of the switching frequency to mitigate circulating current

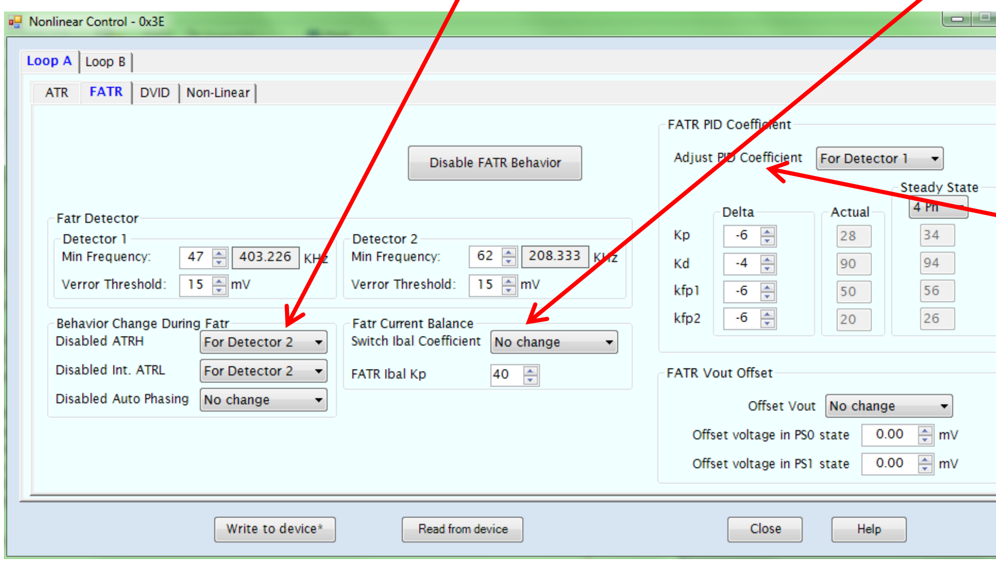
FATR PID Coefficient

–Reducing the PID coefficients during load transient will help stabilize the system

–**Adjust PID Coefficient**
- adjust PID coefficient based on the detector selected

–**Kp/Kd/Kfp**

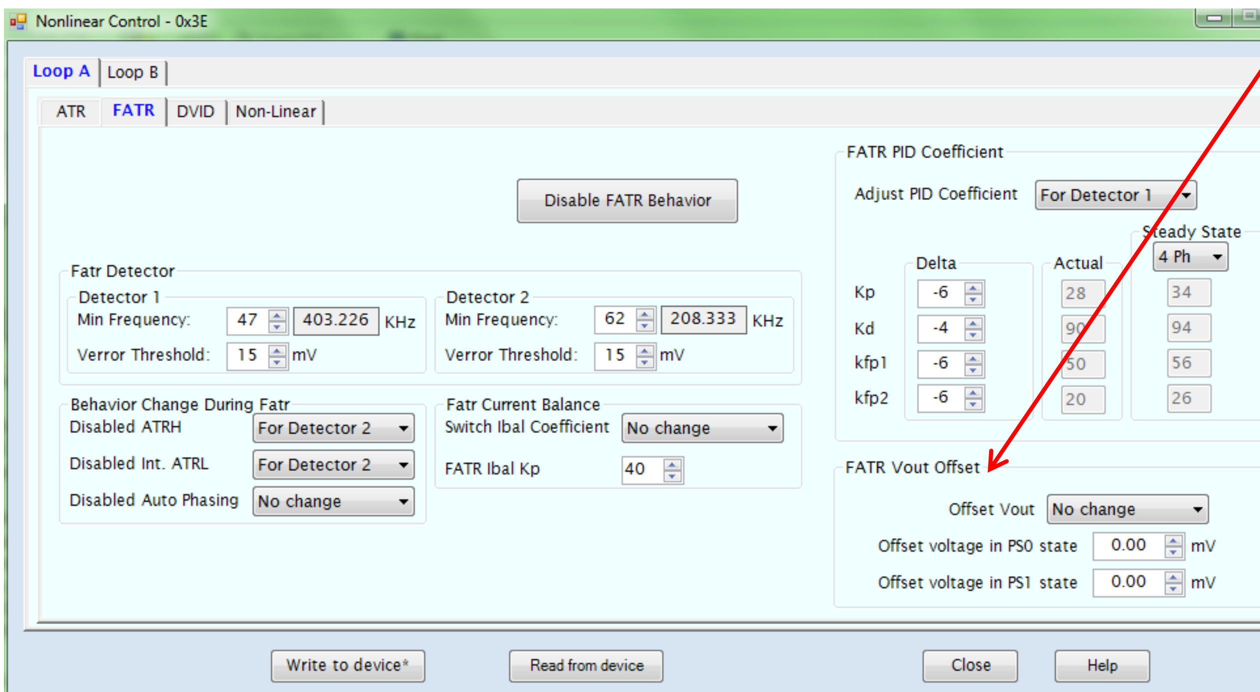
- **Delta**: allows user to set PID coefficient changes
- **Actual**: Calculated value based on the Delta and Steady State
- **Steady State**: Steady state values for the 1Ph, 2Ph, or MaxPh



Nonlinear Control...FATR

FATR Vout offset

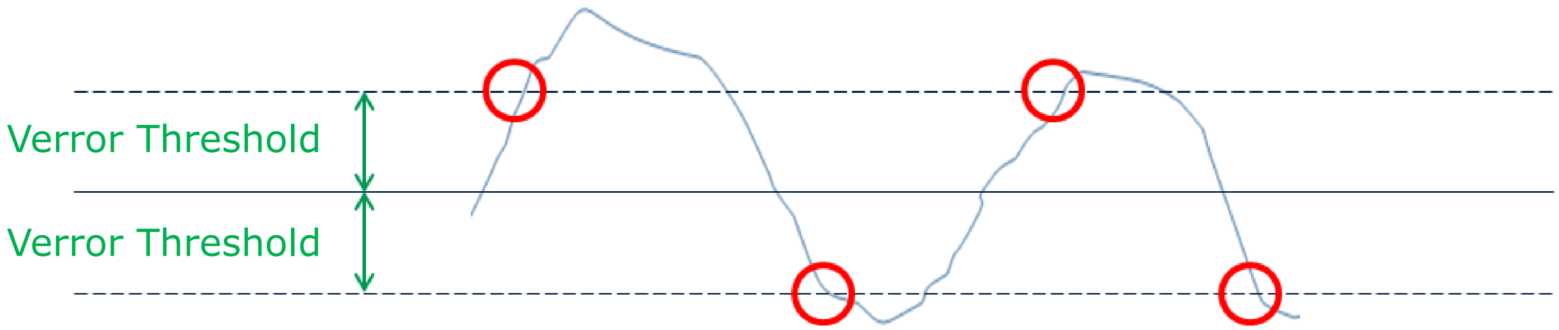
Allows offset compensation that in some conditions can occur when FATR is active



Nonlinear Control: FATR

Verror Threshold (Detector 1/2)

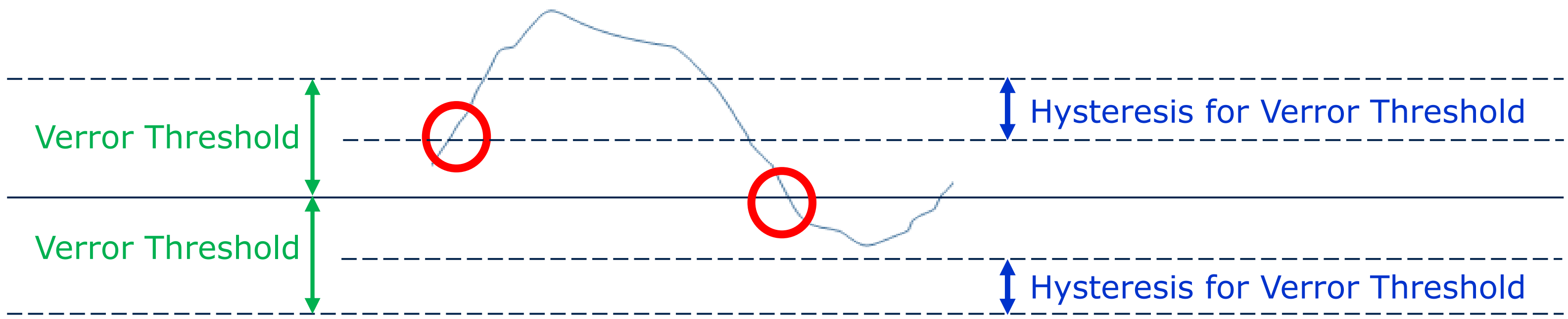
- Defines the window which the controller counts the number of crossings above and below the Verror threshold over time to determine the load repetition frequency
- Verror threshold should be greater than the output ripple voltage to avoid false detection



Nonlinear Control: FATR

Hysteresis for Verror Threshold

- Once the load repetition frequency has been detected, the hysteresis threshold reduces the threshold necessary to stay at the detected frequency



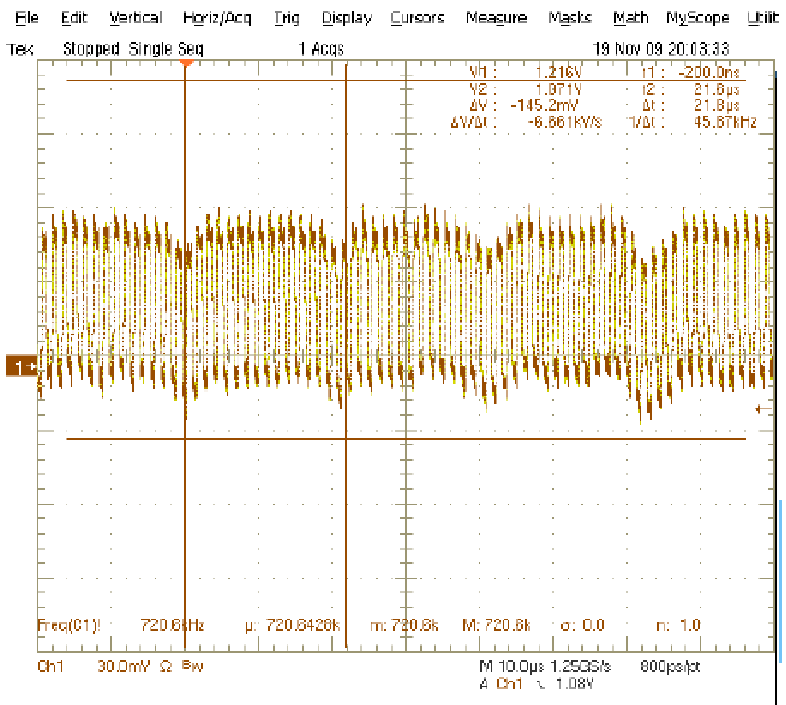
Behavior Change During FATR: select the desired behavior for various Non-Linear features when the load frequency is above the FATR setting

- *No Change*: no behavior change
- *For Detector 1/2/3*: behavior change based on the detector value selected
- ATRH Disabled Rate
  - Rate that applies to both entering and exiting the behavior
  - Recommended settings is Slew

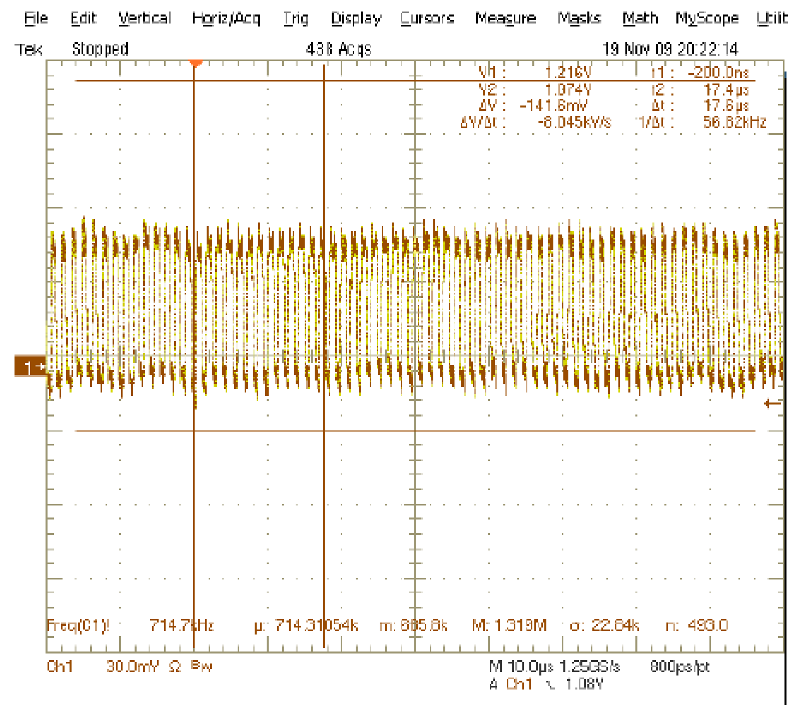
Nonlinear Control: FATR Design Example

- Observation: V_{OUT} oscillation at load frequencies above 700kHz
- Optimization: Reduce PID in FATR PID Coefficient for load frequencies > 700kHz

*FATR **dis**abled*



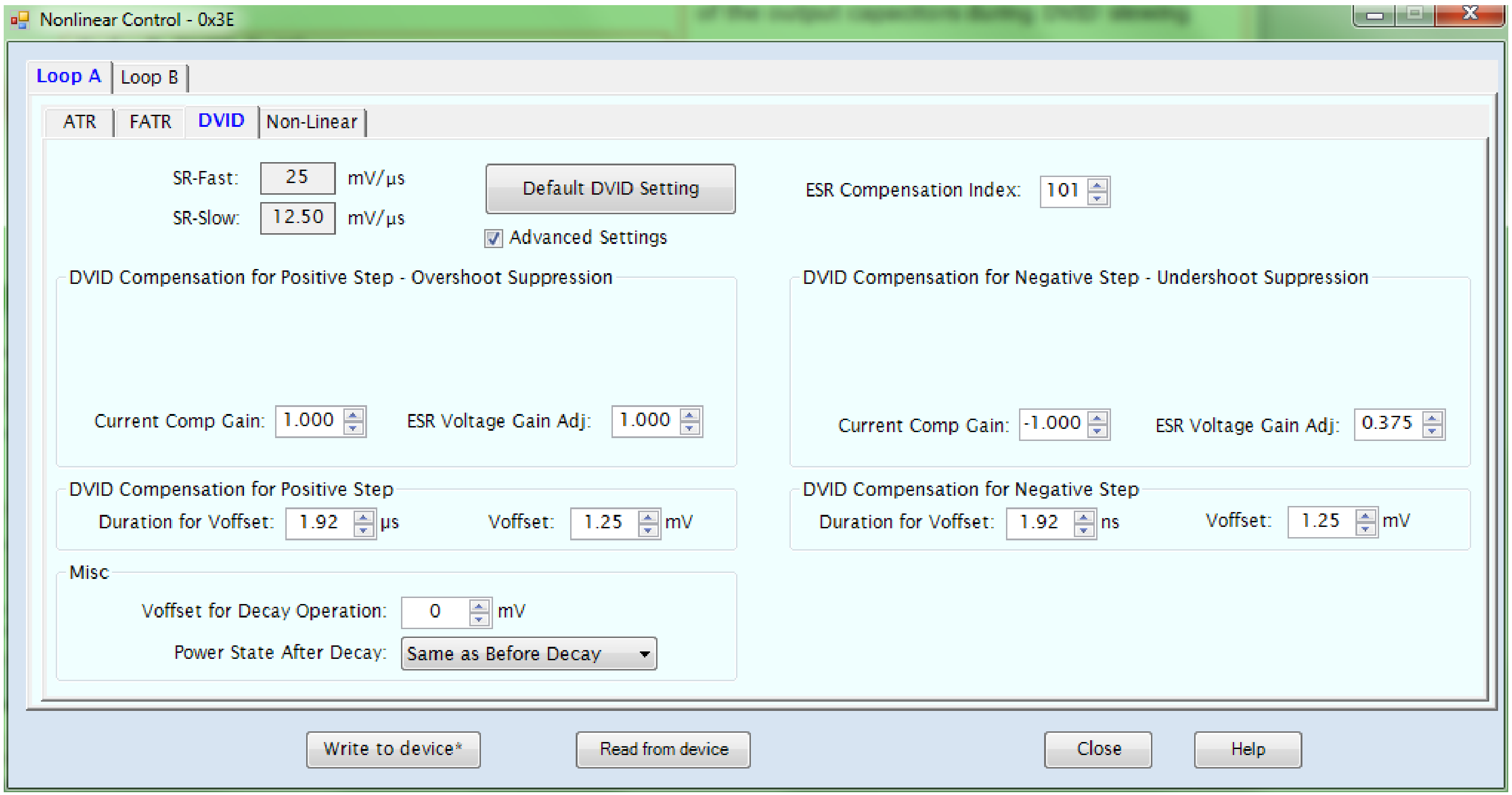
*FATR **en**abled*



VOUT Waveform Comparison

Nonlinear Control…DVID

Dynamic VID (DVID) parameters to optimize the VR's response to the SetVID_Fast/Slow/Decay commands



Nonlinear Control...DVID

Show Advanced Settings
–Enables DVID advance settings when selected

Default DVID Settings

–Calculates and sets the ESR Compensation Index based on the user-specified parameters in the Feedback Loop/Output Model dialog

–Sets all other parameters (including advanced setting parameters) to their default values

ESR Compensation Index

–Calculates the voltage offset caused by the ESR of the output capacitors during DVID slewing

–Is inversely proportional to the Cout *ESR time constant (***Cannot equal 0!***)

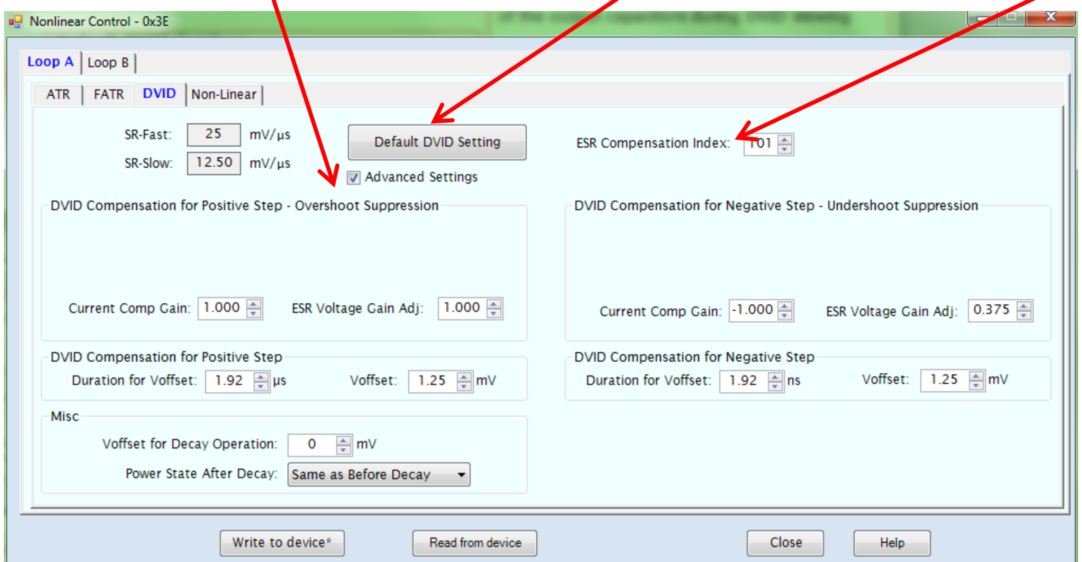
–Decrease and re-adjust the DVID Compensation slider bars (when Advance setting box is not marked)

- If fast response is needed or ring back follows the overshoot
- Lowering this value forces the target voltage to ramp up/down faster that makes the response more aggressive and bigger overshoot if the sliders stay in the same position

–Increase and re-adjust the DVID Compensation slider bars when Advance setting box is not marked

- If there is a need to weaken the compensation

Note: The normal range for **ESR Compensation Index** is ~40 to ~130. Values below 40 often result in a very aggressive response and the ones bigger than 130 end up very small improvements.



Nonlinear Control...DVID

DVID Compensation slider bars

–Use to adjust Current Comp. Gain and ESR Voltage Gain Adjust in positive or negative step

–Positive Step – Overshoot Suppression

•If the DVID response is slow, move the slider to the right to make it faster at the expense of a higher overshoot

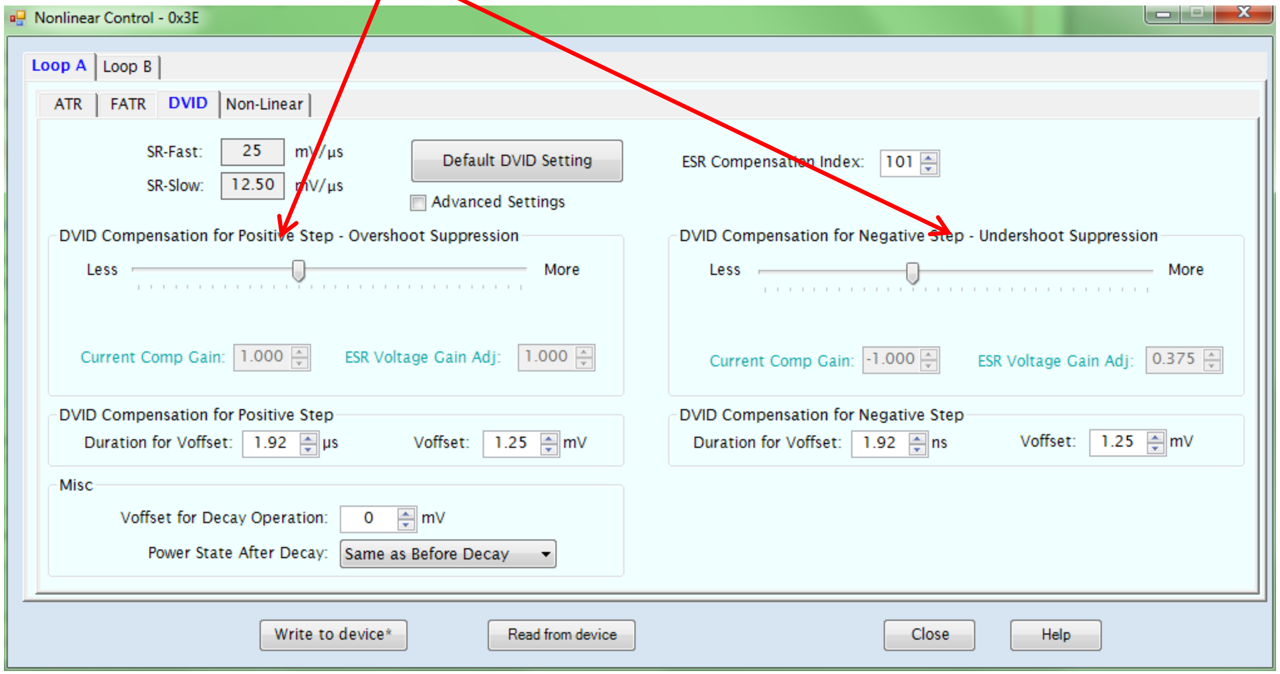
•If the DVID response is very aggressive, move the slider to the left to make it slower and have more overshoot suppression

–Negative Step – Undershoot Suppression

•If a slower response and with less undershoot is desired, move the slider to the left (smaller index)

•Move the slider to the right or left to obtain the desired response

–Slider bars are disabled and not visible when Advance Settings box is marked



Nonlinear Control...DVID

Current Comp. Gain
–Use to compensate the voltage offset caused by the load-line effect on the output capacitor charging or discharging current during DVID slewing
–Directly proportional to load-line and inversely proportional to ESR

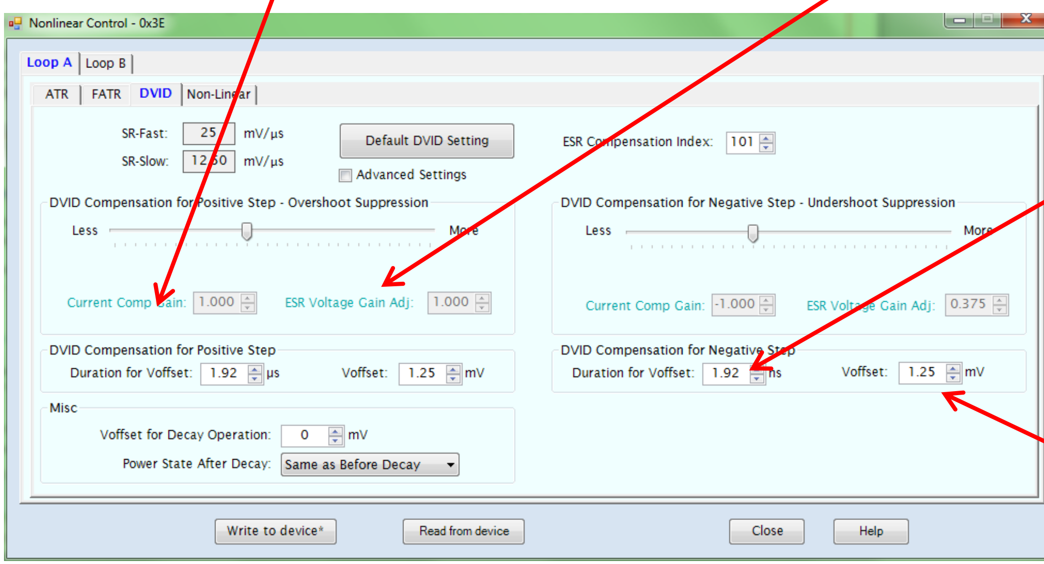
–Positive Step – Overshoot Suppression
•Usually ≥ 1 because faster response is desired

– Negative Step – Overshoot Suppression
•Usually ≤ 0 because response should be slowed down to prevent any undershoot, therefore it is suggested to be not fully compensated

ESR Voltage Gain Adj
–Used to compensate voltage offset caused by the output capacitors' ESR during DVID slewing

–Positive Step – Overshoot Suppression
•Usually set to 1

–Negative Step – Undershoot Suppression
•Usually set less than Positive Step – Overshoot Suppression value

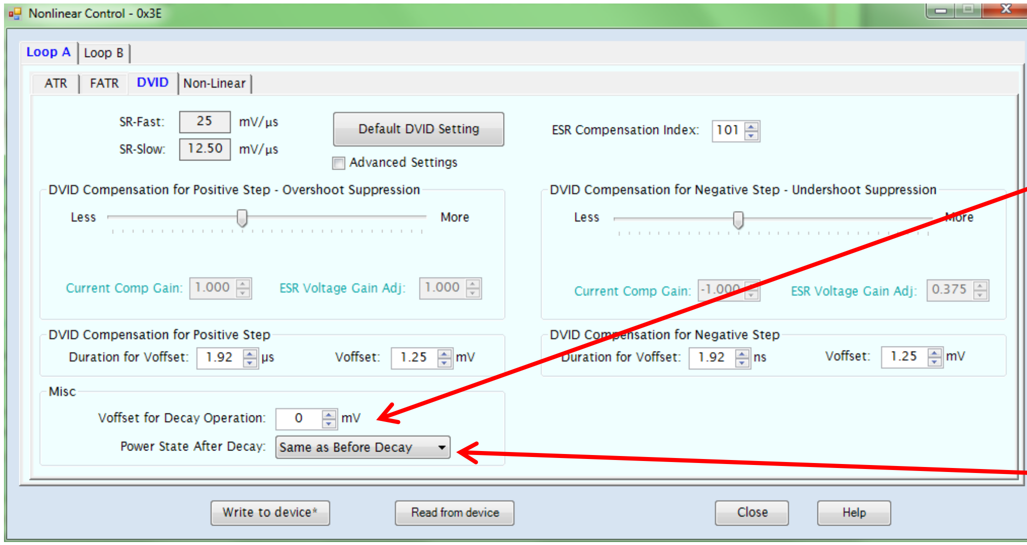


Duration for Voffset

–Time where the Voffset will be applied after the ramp completion
–Independent settings for Positive and Negative Step

Voffset
–Offset amplitude added after the ramp completion
–Independent settings for Positive and Negative Step

Nonlinear Control…DVID



Voffset for Decay Operation

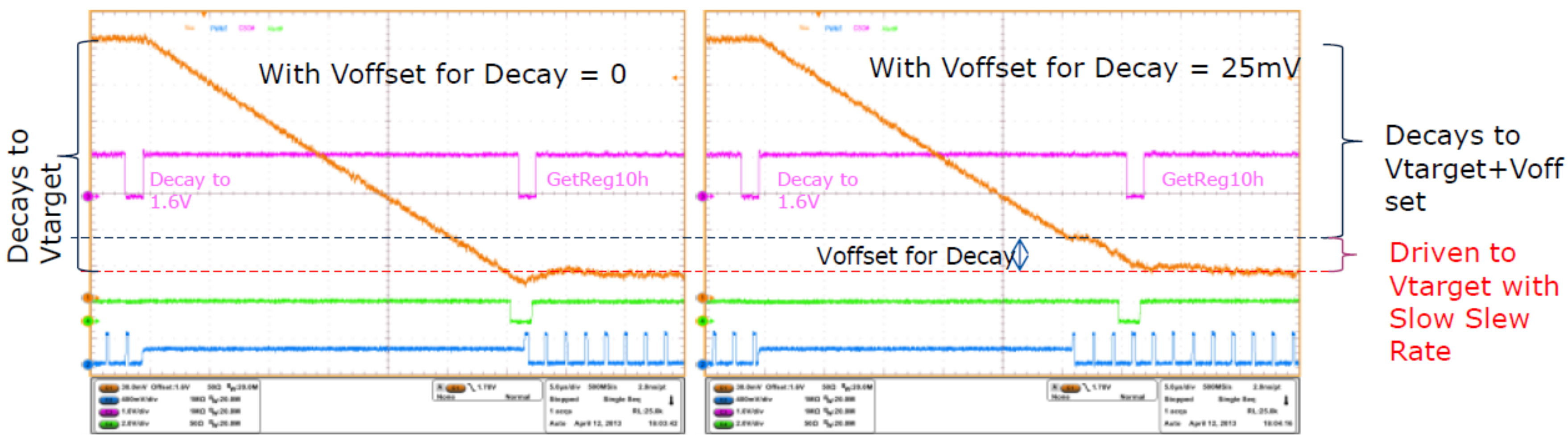
–After the VR reaches the Vtarget + Voffset through decay, the VR will actively drive Vout and continue to ramp to the Vtarget with the specified number of phases for PS2, at slow slew rate

–Recommended value is 25mV

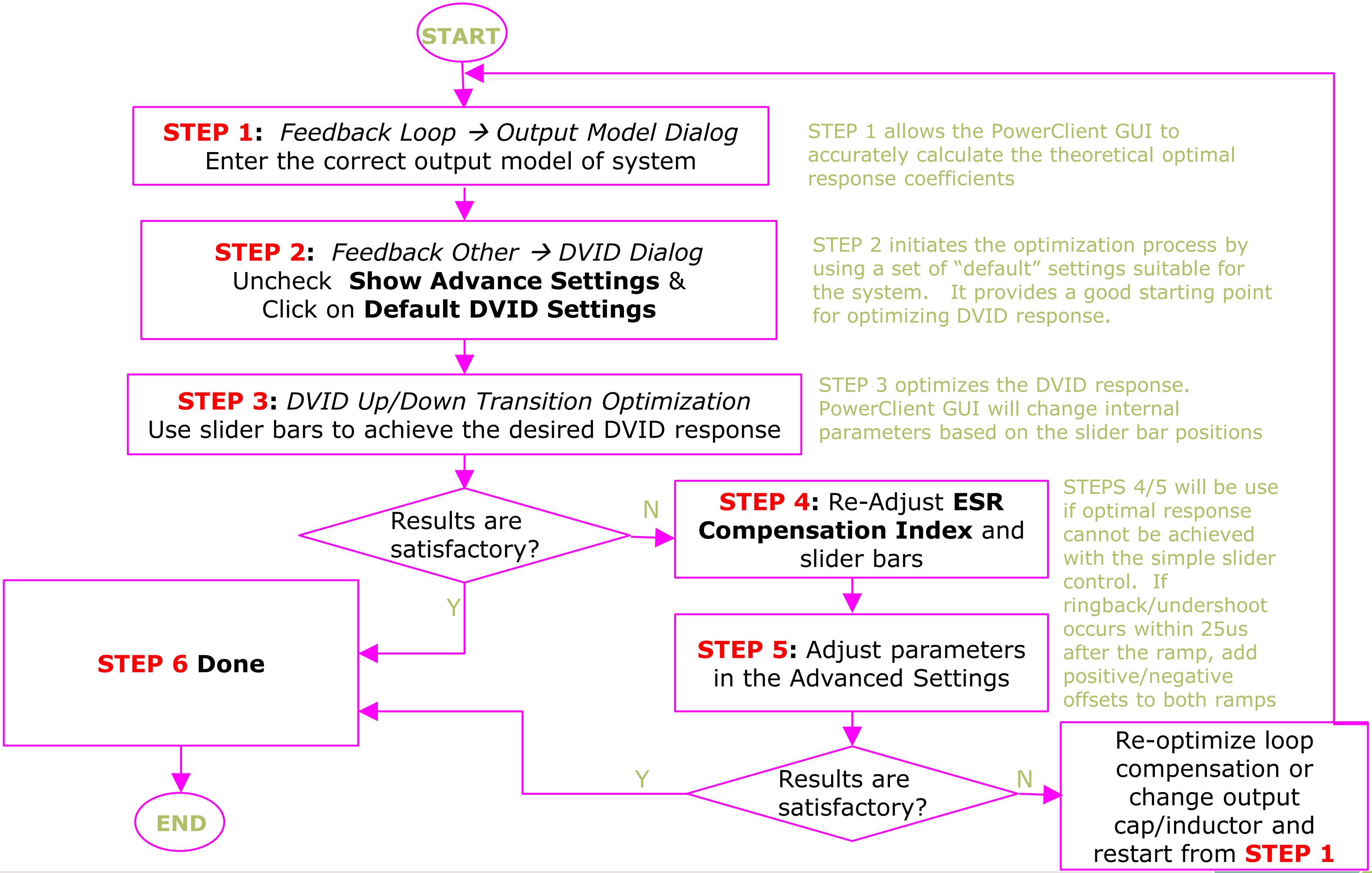
PowerState After Decay

–Same as Before Decay – VR will keep the same PowerState after the decay as it had before decay. Normally for VR13 applications.

–PS2 – VR enters PS2 state after decay. Normally for IMVP8 applications.



Nonlinear Control...
DVID Optimization Procedure

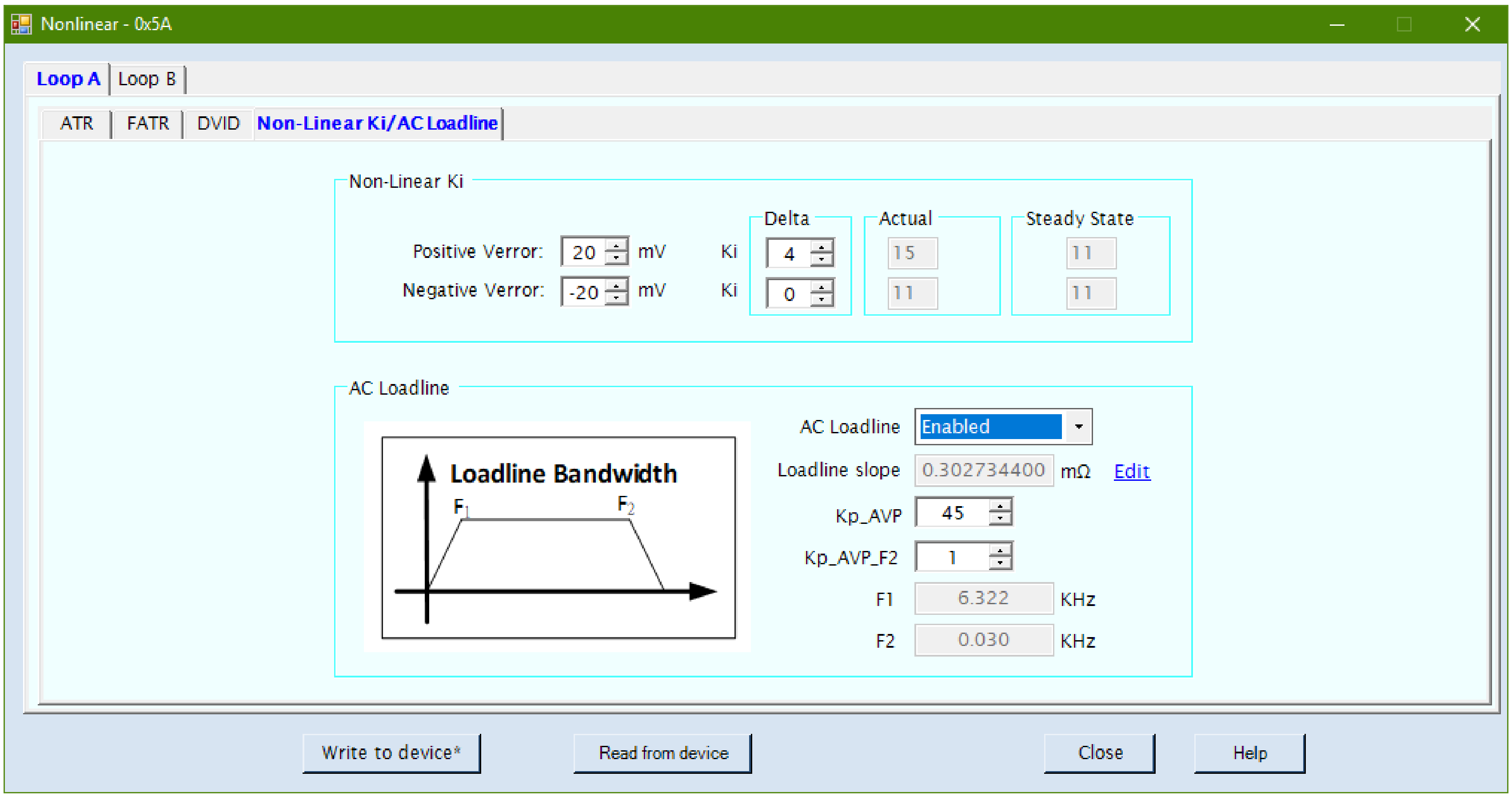


Nonlinear Control...
DVID Optimization Procedure

- If desired response cannot be achieved in **Step 5**
- –Re-adjust PID coefficients in the Feedback Loop/Compensation tab dialog. The current response is not well optimized.
- •An unstable system will cause undesired rings or oscillations
- •A very slow system cannot meet DVID timing requirements
- –Reduce output inductance or capacitance: Current introduced by very large output capacitance (C*dv/dt) is very difficult to compensate for.
- •Extra current (energy stored in L) during a DVID up event will transfer to the output cap resulting in overshoot waveform
- •Large overshoot will accumulate more error in the PID which the loop has to remove, resulting in slight undershoot

Nonlinear Control… Non-linear

Non-Linear parameters to gain more undershoot or overshoot margin at high load repetition frequency. More explanation on next pages.

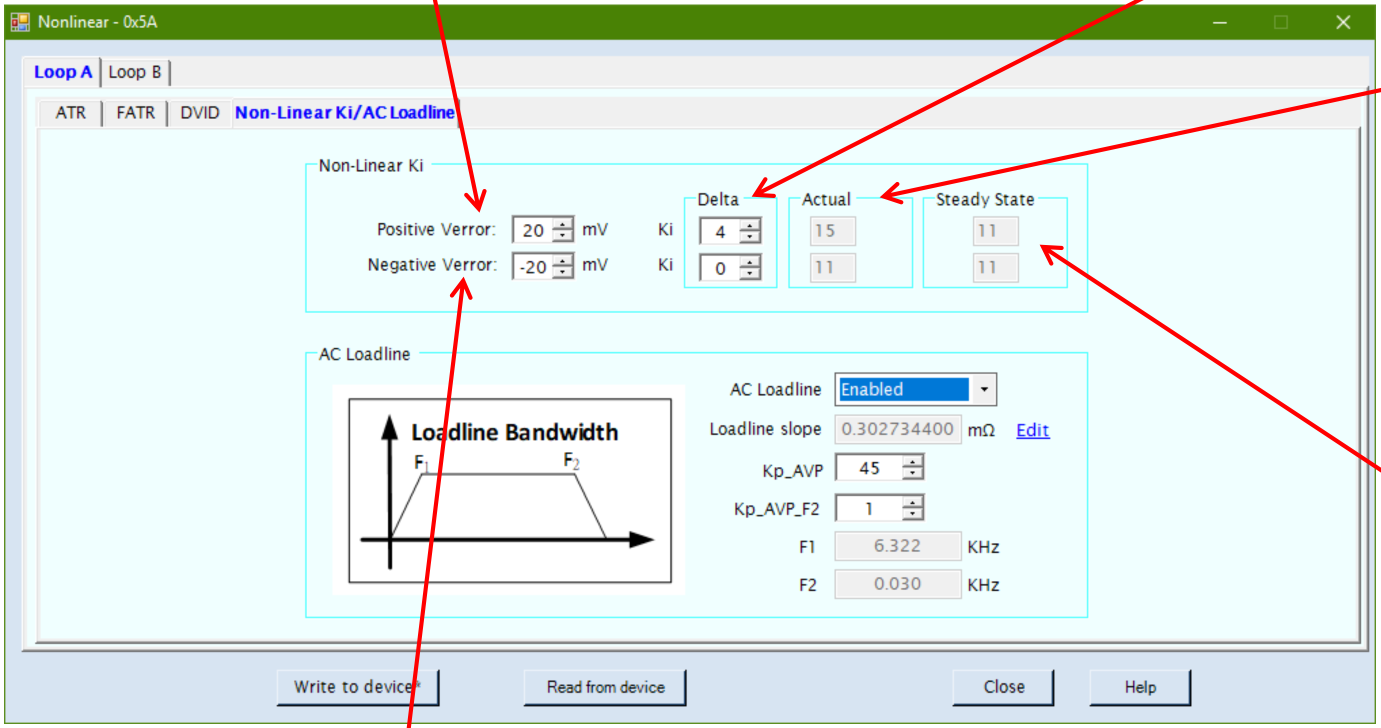


Nonlinear Control… Non-linear

Positive Verror:
–Verror threshold to activate Ki change specified in Delta Ki

Delta Ki :
–Ki change applied to the original Ki when Positive or Negative Verror is met

Actual:
–Calculates and displays the actual Ki when the changes in **Delta** are applied

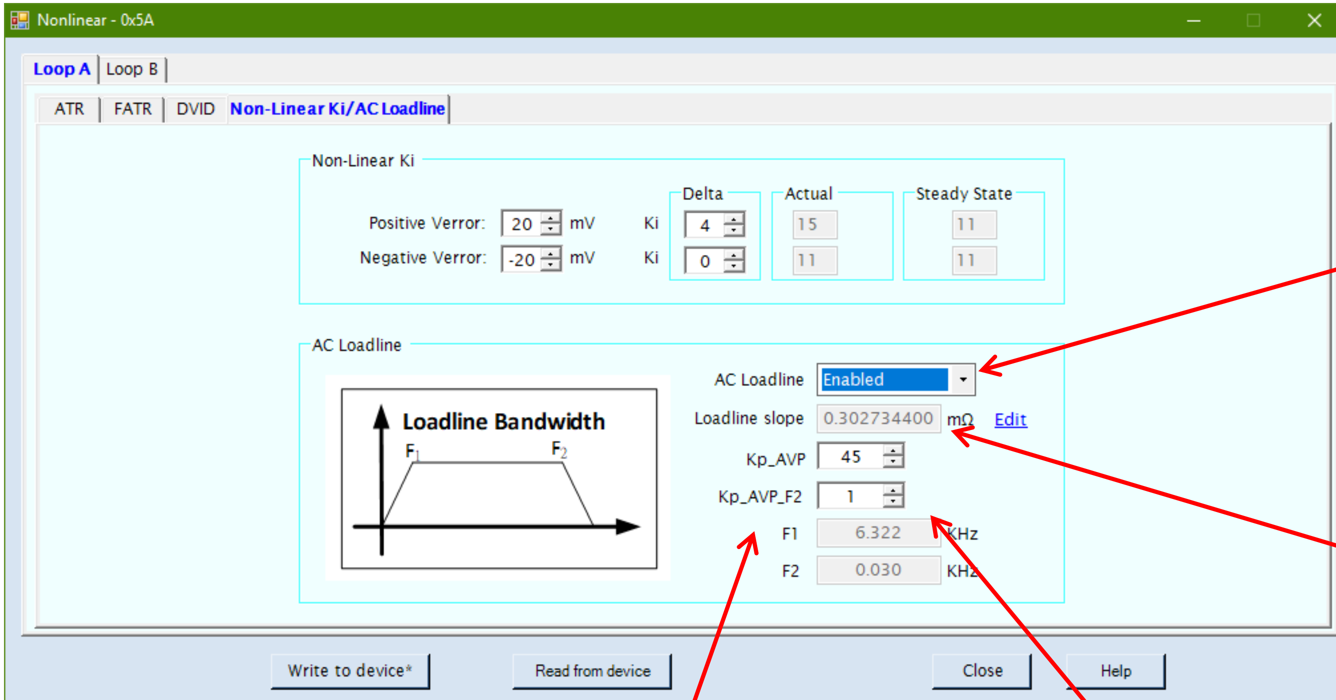


Steady State:
–Displays the original steady state Ki

Negative Verror:
–Verror threshold to activate Ki change specified in Delta Ki

Note: Verror threshold should be larger than output ripple amplitude to avoid false trigger

Nonlinear Control… AC loadline



AC loadline:
Enable or Disable the AC loadline function.
AC loadline add a slope to a loadline between 2 frequencies. While still having the regular performance at steady load for applications that normally do not use loadline.
AC loadline <u>may</u> improve higher frequency load transients to have less over/undershoot.

Loadline slope:
Slope of the AC loadline between selected frequencies.
Notice that when AC loadline is enabled there is no loadline at lower frequencies.

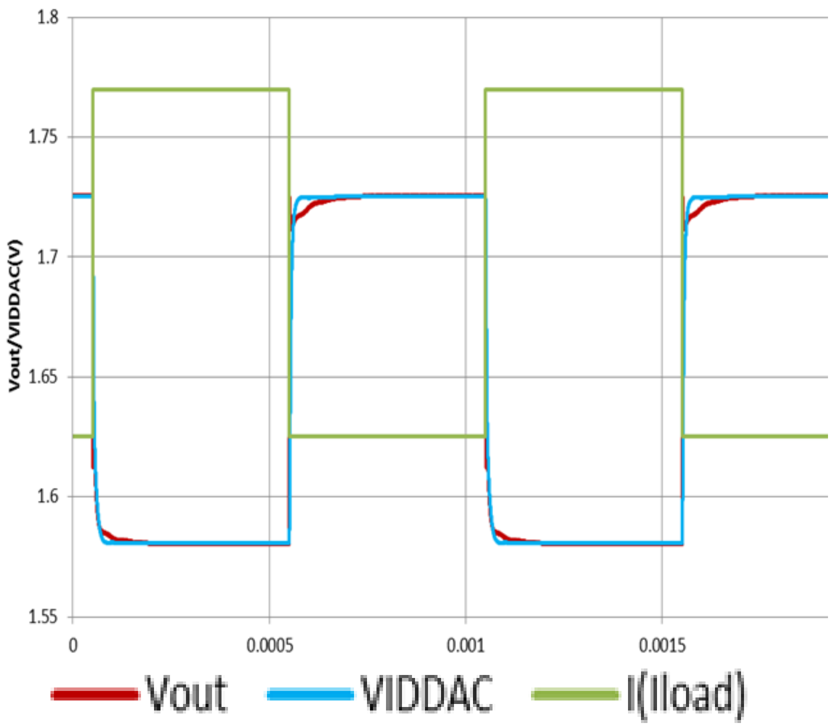
Kp_AVP:
Propotional gain factor at upper frequency of the range where AC loadline works. See calculated frequency F1

Kp_AVP_F2:
Propotional gain factor at lower frequency of the range where AC loadline works. See calculated frequency F2

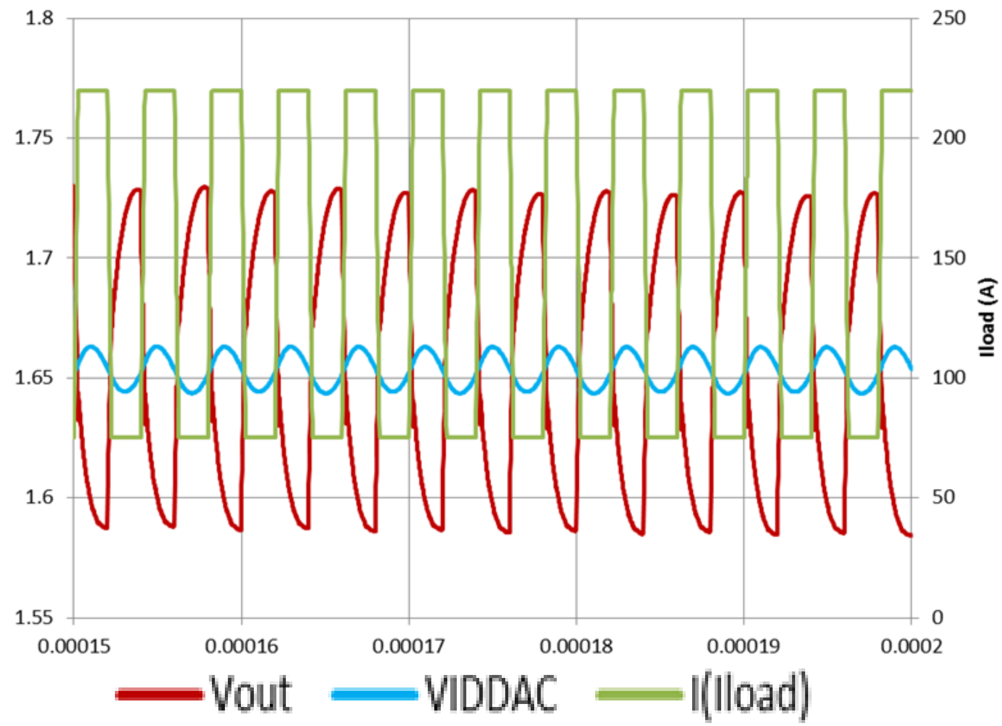
Nonlinear Control:
Non-Linear Background

› At high load repetition frequency, VOUT cannot settle within one load cycle

1kHz Load Transient
(VOUT is settled)



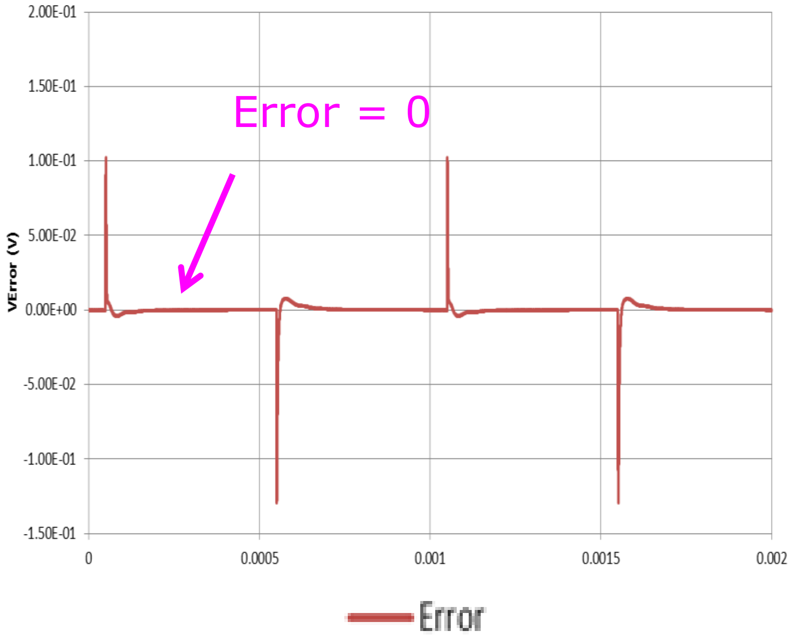
250kHz Load Transient
(VOUT is not settled)



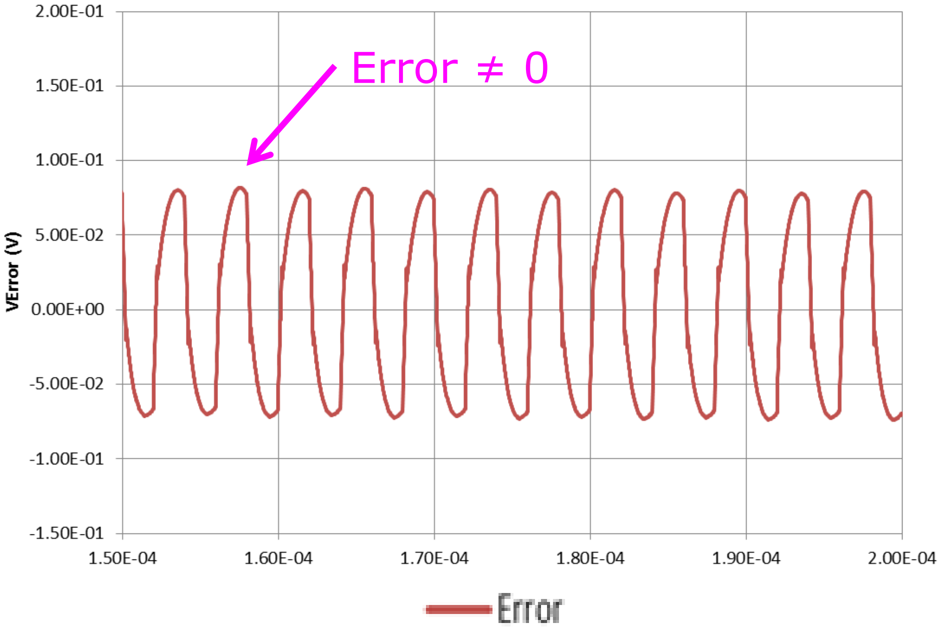
Nonlinear Control:
Non-Linear Background

- For high frequency transient response the error can not be reduced to 0 before next cycle of transient load occurs

VError at 1kHz Load Transient



VError at 250kHz Load Transient

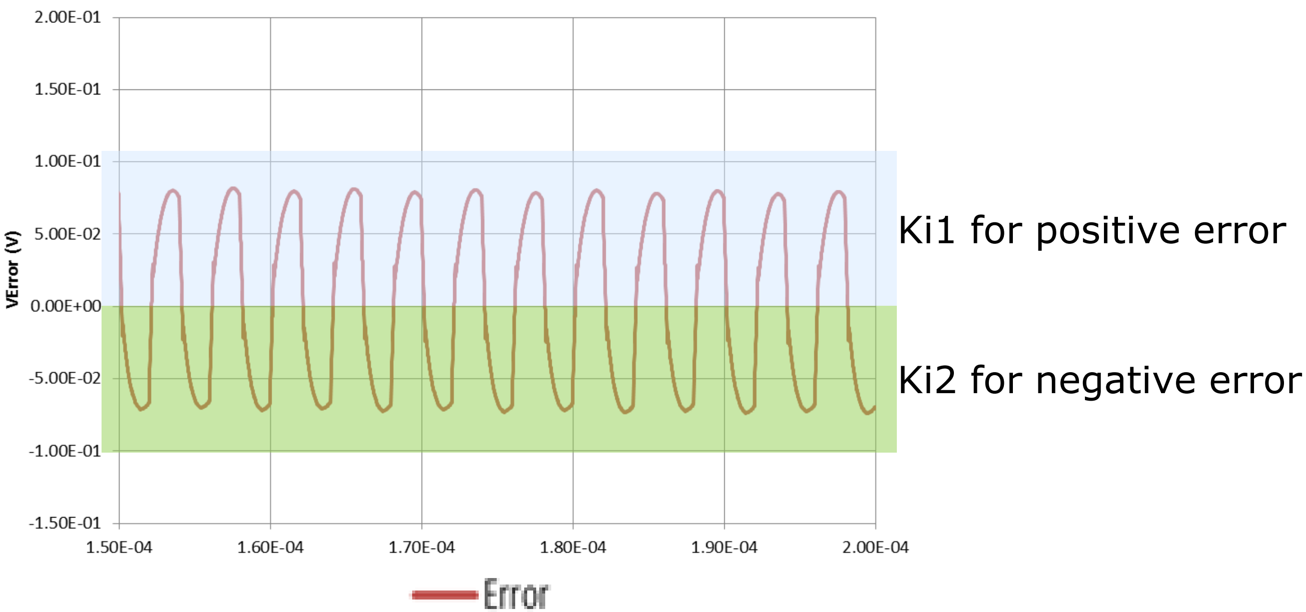


Nonlinear Control: Non-Linear Background

- Compensator I term is proportional to the integrated error

$$I\ term = Ki * \int Error\ dt$$

- Ki for positive and negative Verror can be specified separately to influence the I term:
  - If Ki1 > Ki(original) AND Ki2 ≤ Ki(original), VOUT will be shifted up
  - If Ki1 ≤ Ki(original) AND Ki2 > Ki(original), VOUT will be shifted down



Nonlinear Control: Non-Linear example

› If more undershoot margin is needed, we can specify a positive Ki to shift VOUT up